

Application Note

July 24, 2007

AN1281.1

6A Dual Synchronous Buck Regulator with Integrated MOSFETs

The ISL65426EVAL1Z is a high efficiency dual output monolithic synchronous buck converter operating over an input voltage range of 2.375V to 5.5V. This single chip power solution provides two output voltages, which are selectable or externally adjustable from 1V to 80% of the supply voltage while delivering up to 6A of total output current. The two PWMs are synchronized 180° out of phase reducing the RMS input current and ripple voltage.

The ISL65426EVAL1Z switches at a fixed frequency of 1MHz and utilizes current-mode control with integrated compensation to minimize the size and number of external components and provide excellent transient response. The internal synchronous power switches are optimized for good thermal performance, high efficiency, and eliminate the need for an external Schottky diode.

A unique power block architecture allows partitioning of six 1A capable blocks to support one of four configuration options. One master power block is associated with each synchronous converter channel. Four floating slave power blocks allow the user to assign them to either channel. Proper external configuration of the power blocks is verified internally prior to soft-start initialization.

Independent enable inputs allow for synchronization or sequencing soft-start intervals of the two converter channels. A third enable input allows additional sequencing for multi input bias supply designs. Individual power good indicators (PG1, PG2) signal when output voltage is within regulation window.

The ISL65426EVAL1Z integrates protection for both synchronous buck regulator channels. The fault conditions include overcurrent, undervoltage, and IC thermal monitor.

High integration contained in a thin Quad Flat No-lead (QFN) package makes the ISL65426EVAL1Z an ideal choice to power many of today's small form factor applications. A single chip solution for large scale digital ICs, like field programmable gate arrays (FPGA), requiring separate core and I/O voltages.

Features

High Efficiency: Up to 95%

Fixed Frequency: 1MHz

Operates From 2.375V to 5.5V Supply

• ±1% Reference

Flexible Output Voltage Options

- Programmable 2-Bit VID Input

- Adjustable Output From 0.6V to 4.0V

User Partitioned Power Blocks

• Ultra-Compact DC/DC Converter Design

• PWMs Synchronized 180° Out of Phase

· Independent Enable Inputs and System Enable

• Stable All Ceramic Solutions

• Excellent Dynamic Response

· Independent Output Digital Soft-Start

· Power Good Output Voltage Monitor

Short-Circuit and Thermal-Overload Protection

Overcurrent and Undervoltage Protection

· Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- FPGA, CPLD, DSP, and CPU Core and I/O Voltages
 - Xilinx Spartan III™, Virtex II™, Virtex II Pro™, Virtex 4™
 - Altera Stratix™, Stratix II™, Cyclone™, Cyclone II™
 - Actel Fusion™, LatticeSC™, LatticeEC™
- Low-Voltage, High-Density Distributed Power Systems
- · Point-of-Load Regulation
- Distributed Power Systems
- · Set-Top Boxes.

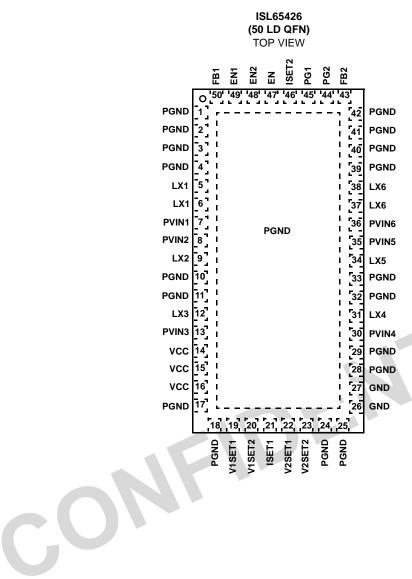
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL65426HRZ*	ISL65426 HRZ	-10 to +100	50 Ld QFN	L50.5x10
ISL65426IRZA*	ISL65426 IRZ	-40 to +85	50 Ld QFN	L50.5x10

^{*}Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout





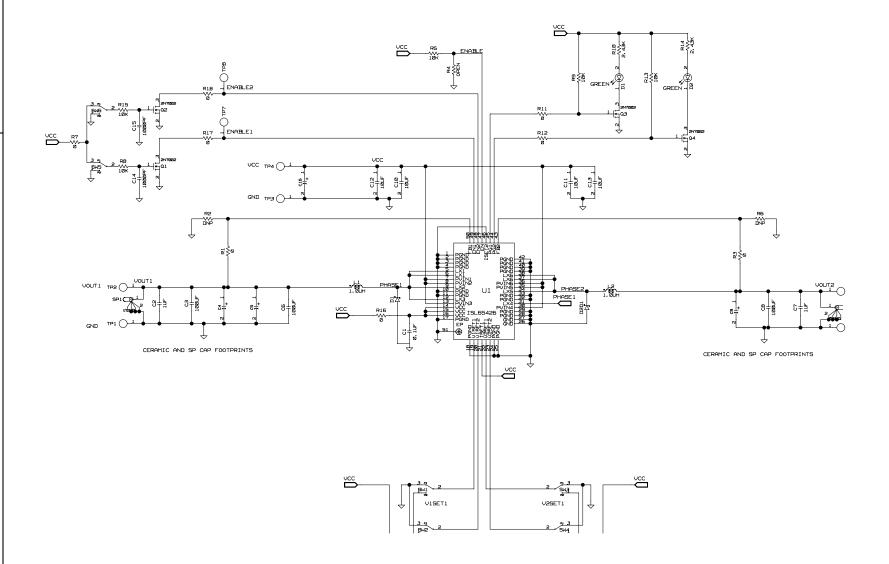


FIGURE 1. ISL65426EVAL1Z REV A CIRCUIT SCHEMATIC

TABLE 1. SWITCH TABLE

Recommended Equipment

- 0V to 6V power supply with at least 10A source current capability, battery, or notebook AC adapter.
- Two electronic loads capable of sinking current up to 5A.
- Digital multimeters (DMMs).
- 100MHz quad-trace oscilloscope.

Quick Start

- Ensure that the circuit is correctly connected to the supply and loads prior to applying any power.
- 2. Turn on the input power supply.
- 3. Turn on EN1 and EN2.
- 4. Verify the outputs voltages are correct based following Table 2:

TABLE 2. OUTPUT VOLTAGE PROGRAMMING

VOUT1	V1SET1	V1SET2	VOUT2	V2SET1	V2SET2
1.8V	1	1	3.3V	1	1
1.5V	0	1	2.5V	0	1
1.2V	1	0	1.8V	1	0
0.6V	0	0	0.6V	0	0

- 5. Load VOUT1 up to 4A.
- 6. Load VOUT2 up to 2A.

Application Note 1281

ISL65426EVAL1Z BOM

REF DES	QTY	PART NUMBER	VALUE	DESCRIPTION	MANUFACTURER
C1	1		0.1µF	Ceramic Capacitor, 16V, 10%, X7R, 0603	various
C10, C11, C12, C13	4		10µF	Ceramic Capacitor, 6.3V, 20%, X7R, 1206	various
C14, C15	2		1000pF	Ceramic Capacitor, 50V, 10%, X7R, 0603	various
C16	0	UHN0J222MPP	2200µF	Electrolytic Capacitor, 6.3V, 20%, thru-hole	Nichicon
C2, C7	2		1µF	Ceramic Capacitor, 10V, 10%, X5R, 0603	various
C3, C6, C8	3	C3225X5R0J107M	100µF	Ceramic Capacitor, 6.3V, 20%, X5R, 1210	TDK
C4, C5, C9				SP Cap Place Holder	
D1, D2	2	LTST-C170CKT		Green LED, 0805	
L1, L2	2	FDV0630-1R0M	1.0µH	Power Inductor, 20%, 7.7A, 10mΩ DCR, SMD	токо
Q1, Q2, Q3, Q4	4	2N7002		N-Channel MOSFET, 60V, 115mA,SOT23	various
R1, R3, R7, R11, R12, R17, R18	7		Ω0	Chip Resistor, 0603	various
R10, R14	2		2.43kΩ	Chip Resistor, 0603	various
R16	1		5Ω	Chip Resistor, 0603	various
R2, R6			DNP	Chip Resistor, 0603	various
R4	1		2.21kΩ	Chip Resistor, 0603	various
R5, R8, R9, R13, R15	5		10kΩ	Chip Resistor, 0603	various
SP1, SP2	2	1314353-00		Probe Socket, Thru Hole	Tektronics
SW1, SW2, SW3, SW4, SW5, SW6	6	GT11MSCKE		Toggle Switch, Mini SPDT, SMD	C&K
TP1, TP2, TP3, TP4, TP5, TP6	6	1514-2		Turret Test Point, Thru Hole	Keystone
TP7, TP8	2	SPCJ-123-01		Small Test Point, Thru Hole	Jolo
U1	1	ISL65426CRZ		Dual Controller 50 Ld QFN	Intersil
CC					

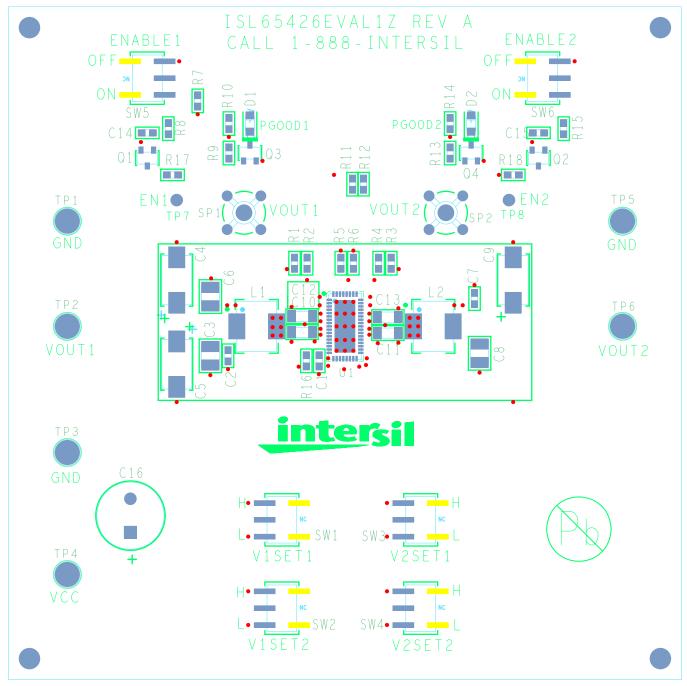


FIGURE 2. TOP LAYER COMPONENTS

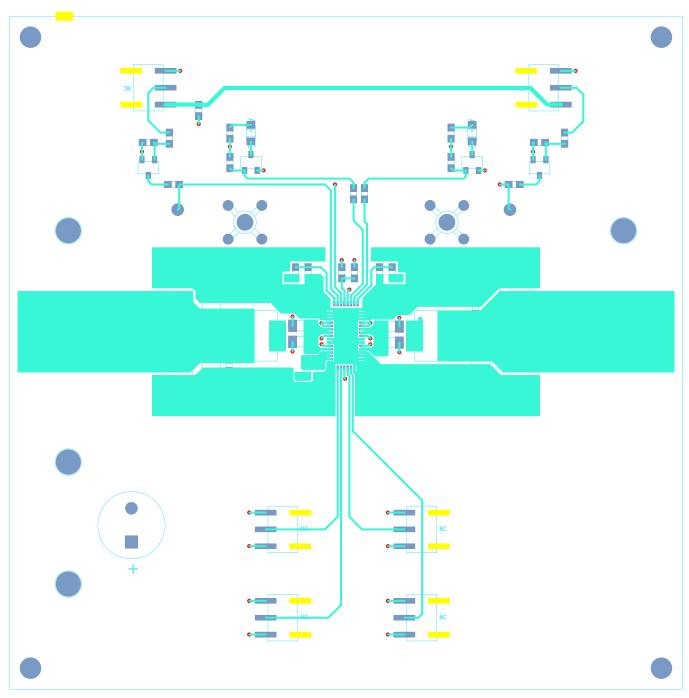


FIGURE 3. TOP LAYER ETCH

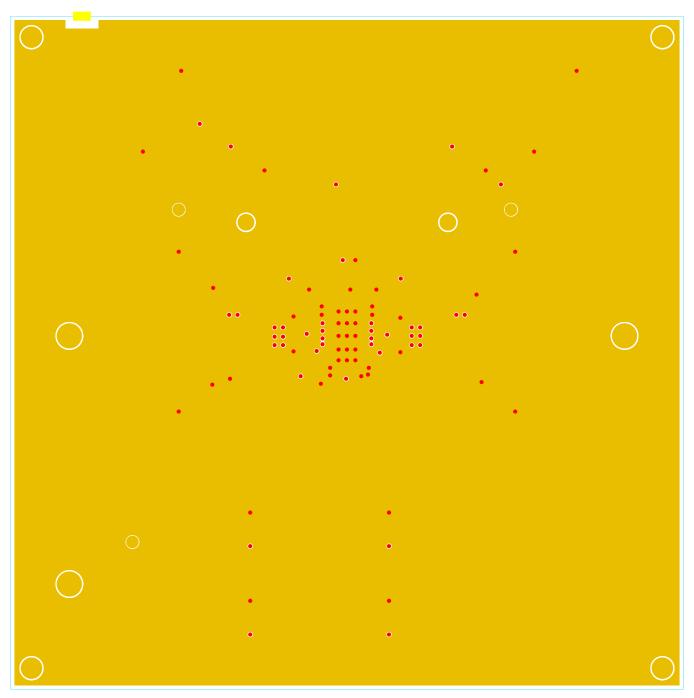


FIGURE 4. SECOND LAYER ETCH

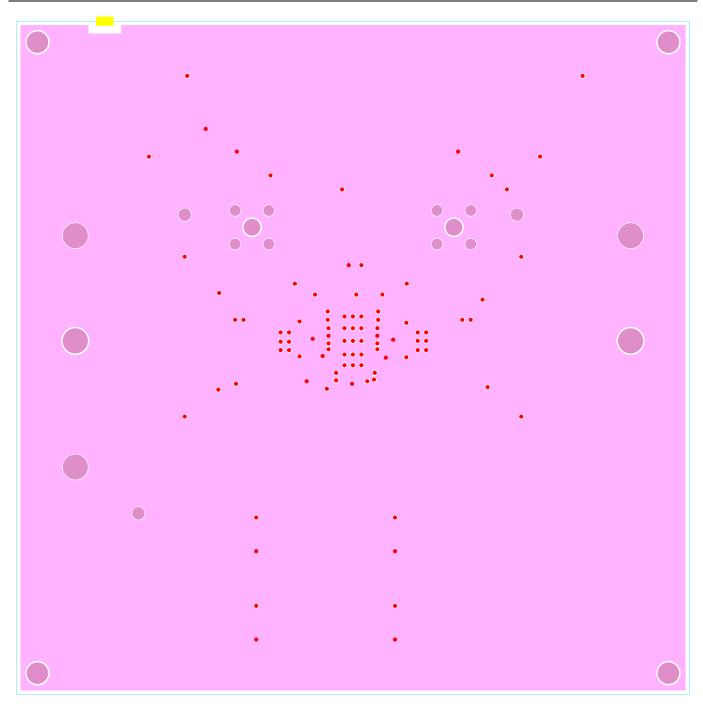


FIGURE 5. THIRD LAYER ETCH

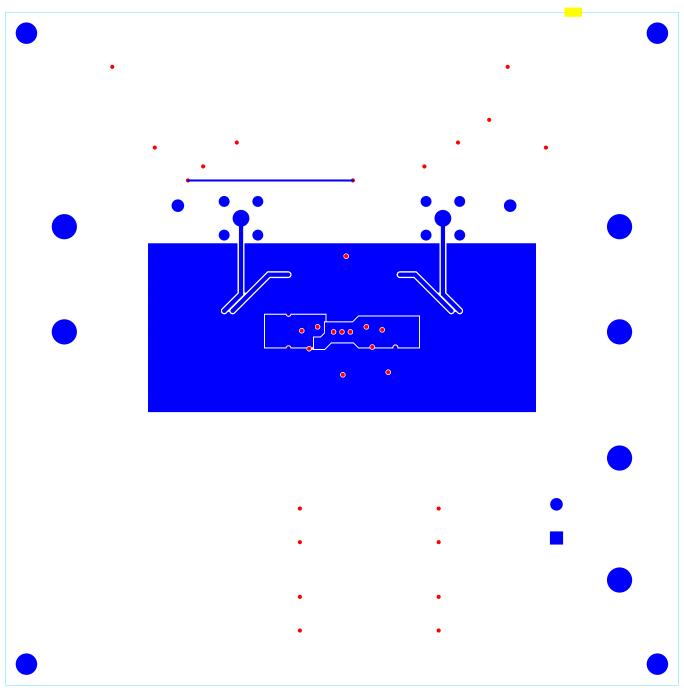


FIGURE 6. BOTTOM LAYER ETCH (MIRRORED)

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